Remarks:

Reconsideration of the application is requested.

Claims 1-12 remain in the application. Claims 10-12 have been withdrawn.

In the third paragraph on page 2 of the Office action, claims 1-3, and 5-9 have been rejected as being obvious over Leung et al. (U.S Patent No. 5,563,762) in view of Matsuoka et al. (U.S Patent No. 6,130,449) under 35 U.S.C. § 103.

In the second paragraph on page 4 of the Office action, claim 4 has been rejected as being obvious over Leung et al. (U.S Patent No. 5,563,762) in view of Matsuoka et al. (U.S Patent No. 6,130,449) and in further view of Kuroiwa et al (U.S Patent No. 6,239,460 B1) under 35 U.S.C. § 103.

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and the claims have, therefore, not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

"said third metal area together with said dielectric layer and said first metal area forms a memory element"

The Examiner has maintained his rejection of claim 1 of the instant application, based on the argument that high density devices as shown by the Matsuoka et al. reference require an integration of an upper metallization layer above a capacitor. The Examiner's argument continues that therefore, a person of ordinary skill in the art would place the capacitor of the Leung et al. reference underneath a metallization layer when integrating it into the device of the Matsuoka et al. reference.

Applicants respectfully disagree with this argument for the reasons set forth below.

The Leung et al. reference does not disclose a memory element as claimed in the present invention.

The Leung et al. reference discloses an **on-chip** capacitor that is a discrete component (i.e. a coupling/decoupling capacitor or a filter) (column 1, lines 21-29; column 1, lines 50-55; column 6, lines 26-47; column 11, lines 54-60). The number of

on-chip capacitors is a large number (tens) (column 6, line 38).

Furthermore, the Leung et al. reference discloses that many applications require a capacitance in the nF range (column 11, lines 39-40). Even if a ferroelectric material were to be used (using thin films of PZT, a capacity of greater than 30 $fF/\mu m^2$ was achieved) (column 11, lines 49-50), a capacitor having an area of roughly 30,000 μm^2 would be required. Such a capacitor is much larger than a memory capacitor, which is typically in the range of less than a micron.

Also, the Leung et al. reference teaches placing the capacitor on top of the passivation layer of an otherwise completed integrated circuit (column 3, lines 45-48; column 6, lines 26-28). Further, as described in conjunction with Fig. 3, "the substrate 102 comprises a conventionally finished wafer comprising a plurality of completed and passivated integrated circuits" (column 7, line 66 to column 8, line 1). A memory element is typically part of an integrated circuit and is generally not disposed on top of an otherwise completed integrated circuit.

Therefore, the Leung et al. reference does not show a third metal area together with the dielectric layer and the first

metal area forming a memory element, as recited in claim 1 of the instant application.

It is also noted that the capacitor disclosed in the Leung et al. reference is made of metal electrodes and ferroelectric dielectrics (column 4, lines 18-21; column 8, lines 48-59; column 11, lines 30-53 and lines 61-67). Claim 1 of the present invention claims the use of metal for the first through fourth metal areas. Contrary thereto, the Matsuoka et al. reference uses polysilicon as the material for the capacitor electrodes (layer 1021) (column 10, lines 62-66), (layer 1203) (column 12, lines 4-8), and (layer 1204) (column 12, lines 44-50).

Therefore, the integration of metal electrodes into the device of Matsuoka et al. would require a significant alteration of the teachings of the Matsuoka et al. reference. A simple transfer of the capacitor according to the Leung et al. reference into the device of Matsuoka et al. would not be possible without significant modifications of the device according to Matsuoka et al..

Accordingly, when looking at the remarks given above, it is seen that a person of ordinary skill in the art would not combine the teachings of the Leung et al. reference with the teachings of the Matsuoka et al. reference, especially when

considering the scope of the Leung et al reference. As stated in the Office action dated June 7, 2002, the goal of the Leung et al. reference is to place a discrete capacitor on top of the passivation layer of an otherwise completed integrated circuit (column 3, lines 45-47). Therefore, regardless of whether the density of the device according to the Matsuoka et al. reference is high or not, a person of ordinary skill in the art would place the discrete capacitor of the Leung et al. reference on top of any integrated devices.

A critical step in analyzing the patentability of claims pursuant to 35 U.S.C. § 103 is casting the mind back to the time of invention, to consider the thinking of one of ordinary skill in the art, guided only by the prior art references and the then-accepted wisdom in the field. See In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614,1617 (Fed. Cir. 1999). Close adherence to this methodology is especially important in cases where the very ease with which the invention can be understood may prompt one "to fall victim to the insidious effect of a hindsight syndrome wherein that which only the invention taught is used against its teacher." Id. (quoting W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 313 (Fed. Cir. 1983)).

Most if not all inventions arise from a combination of old elements. See In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d

1453,1457 (Fed. Cir. 1998). Thus, every element of a claimed invention may often be found in the prior art. See id. However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. See id. Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the appellant. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 163.5, 1637 (Fed. Cir. 1998); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125,1127 (Fed. Cir. 1984).

The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved. See Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617. In addition, the teaching, motivation or suggestion may be implicit from the prior art as a whole, rather than expressly stated in the references. See WMS Gaming, Inc. v. International Game Tech., 184 F.3d 1339, 1355, 51 USPQ2d 1385, 1397 (Fed. Cir. 1999). The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art. See In re Keller, 642 F.2d 413,

425, 208 USPQ 871, 881 (CCPA 1981) (and cases cited therein). Whether the examiner relies on an express or an implicit showing, the examiner must provide particular findings related thereto. See Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617. Broad conclusory statements standing alone are not "evidence." Id. When an examiner relies on general knowledge to negate patentability, that knowledge must be articulated and placed on the record. See In re Lee, 277 F-3d 1338, 1342-45, 61 USPQ2d 1430, 1433-35 (Fed. Cir. 2002).

Upon evaluation of the Examiner's response, it is respectfully believed that the evidence adduced by the examiner is insufficient to establish a prima facie case of obviousness with respect to the claims.

It is applicants' position that the argument presented by the Examiner, namely that the high density of the device disclosed by Matsuoka et al. would encourage a person of ordinary skill in the art to place the capacitor disclosed by the Leung et al. reference underneath a metallization layer, is an inadmissible hindsight consideration in light of the present invention. A person of ordinary skill in the art would not consider a combination of the Leung et al. reference with the Matsuoka et al. reference. Accordingly, the Examiner is requested to withdraw the rejection.

It is noted that the Kuroiwa et al. reference does not make up for the deficiencies of the Leung et al. and Matsuoka et al. references.

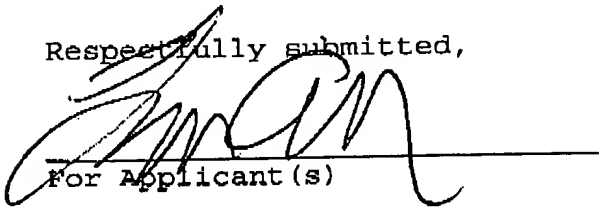
It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-9 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel respectfully requests a telephone call so that, if possible, patentable language can be worked out.

Please charge any other fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner & Greenberg P.A., No. 12-1099.

Respectfully submitted,



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